NAVEEN BHUKYA

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Summary

Highly skilled Electrical Engineer with expertise in VLSI design and verification, proficient in Verilog, System Verilog, UVM, and experienced in RTL coding, test bench development, and FPGA/ASIC design. Strong educational background with a master's in electrical engineering (VLSI Specialization) and a bachelor's in electrical engineering, and practical experience as a VLSI Design and Verification Trainee.

Education

Masters in electrical engineering (Specialization in VLSI) **GPA-3.45**
San Jose State University Jan/2022-Dec/2023
Course Work: Digital Systems Design and Synthesis, Advanced Computer Architecture, UVM and Embedded SOC and Design (ARM-M0)

Bachelor's in electrical engineering **GPA-3.3**
VIT, Vellore, India *June/2017-May/2021*
Course Work: Microprocessor and microcontroller, Analog and digital circuits, problem solving and oops, Electric Vehicle, semiconductor devices and circuits, Automated test engineering, Engineering optimization.

Technical Skill

Hardware Languages	**:** System Verilog**,** Verilog
Methodology	: UVM (Universal Verification Methodology)
Languages	**:** Python, Perl, TCL
Tools	**:** Xilinx Vivado, Quartus Prime, Synopsys (Design Vision, Design Compiler), Matlab, gtkwave, spike.
Protocols	**:** AHB, APB, I2C, UART
Core Skills	**:** RTL coding using Synthesizable constructs of Verilog, Creation of self-checking test bench, Functional Coverage, Assertions, Pipelining, Static Timing Analysis, & CMOS Fundamentals, Instruction set architecture (Arm ,Risc-v, Mips).

Experience

ADVANCED VLSI DESIGN AND VERIFICATION TRAINEE Oct/2021 - Apr/2022
Maven Silicon
Skills acquired on**: Verilog,** Basics of **FPGA,** Basics of **CMOS, System Verilog, UVM, and Static Timing Analysis**, **and Linux.**
Training Projects: **Router 3x1 |Verilog, Dual port ram |System Verilog, UVM, Coverage and Assertions**

Workshop and Certification

VSD-Product based RISC-V Skilling Program Mar/2024-present
VLSI System Design
A comprehensive six-week workshop focusing on mastering the RISC-V Instruction Set Architecture (ISA) , encompassing both theoretical concepts and practical applications.

- Gained in-depth knowledge of RISC-V architecture, Verilog simulations RV32I microarchitecture simulation, Verilog code analysis, real-world I/O implementation strategies, and C code optimization for RISC-V applications.

Academic Projects

AHB2APB Bridge IP Core Verification| System Verilog, UVM, GTKWave (Waveform Visualizer)

- Designed AHB2APB Bridge synthesizable module for communicating an AHB as master and a APB as Slave using System Verilog and done verification using UVM methodology with two agents one for AHB and another for APB. Used handshake method to synchronize communication between AHB and APB using this Bridge and uses HCLK and HRESETn signals in the Bridge.
- Bridge FSM takes care of generation of AHB and APB signals and the address decoding logic which helps to generate APB peripheral select lines.
- Tested scenarios using UVM are reset, burst read and write, Invalid address (Error response handling), Single read and write, read after write, and write after read. Functional coverage is also implemented to ensure the real intent of the design is covered or not.

A Display Controller | system Verilog, **graphics controller**, **Arbitration, FPGA**

- This project uses Synchronous FIFO module (Fixed depth FIFO in each VGA controller module to store pixel data which reads faster from memory and displays slowly), Bus switch module (To handle requests and send data to 3 VGA controllers at a time), Memory module (for pixel data storage), Test bench module, Counter Module and VGA display controller module.
- Test bench module which initiates the transfer by sending control registers to a particular display module to display pixel data and cursor info, Memory module used to get pixel data which need to be displayed by the display modules upon the request of VGA display controller.
- In display controller module, created FSM to push the pixel data coming from memory module and get pixel data from FIFO to display according to its corresponding Counter signals generated by Counter module, and In Bus switch module used **Round Robin** scheduling method to handle three 3 VGA display controllers request at a time.

8250 UART verification | UVM, **Verilog**

- Design has a Baud Clock Generator with different frequencies (such as 9600,14400,38400,57600,115200,128000) and a FSM which converts the data into serial data.
- Architected the class-based verification environment in UVM to ensure proper functionality and performance by developed and integrated UVM components, including sequences, agents, drivers, monitors, and scoreboards, to automate the verification process and improve test coverage.
- Created test benches to simulate different test scenarios like by setting fixed length, random baud, and having 1 stop and two stop bits; and by random length and baud, to ensure the system was working correctly under all conditions and met design specifications and performance requirements.

Fixed Point MAC 3-stage Pipeline | Verilog

- Designed Fixed Point MAC unit using Verilog, it performs MAC operation using two inputs with 8 values each and implemented it with a 4 state FSM (Reset, Input A, Input B, MAC result) for the overall implementation and a 3-stage pipeline methodology for MAC operation on the given inputs for better throughput.
- Hardware components used are Arduino Uno board, 16x2 LCD display (To observe current state), DE 10 Lite FPGA board, Bread board, Connecting wires, and 4x4 Numerical hex keypad.
- Design modules used are BCD to 7-segment decoder (To display inputs and result on FPGA board), Clock divider (different for input and output display), debounce (for push signals to increment address and change state), 2 SRAMS (for two inputs), Pipeline MAC, Hex keypad (To read data from input), FP Multiplier, and FP Adder.